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L6: Entry 5 of 66 File: PGPB Nov 11, 2004

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DOCUMENT-IDENTIFIER: US 20040225758 A1

TITLE: Prefetch control in a data processing system

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INVENTOR-INFORMATION:

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REPRESENTATIVE-FIGURES: 1

ABSTRACT:

A data processing system (10) includes an interconnect (22) where a first interconnect master (12) and a second interconnect master (14) are coupled to the interconnect. A shared storage (35) is coupled to the interconnect for use by the first and second interconnect masters. The data processing system also includes a first control storage circuit (60, 64) which corresponds to the first interconnect master and a second control storage circuit (62, 66) which corresponds to the second interconnect master. In one embodiment, prefetch circuitry (40) is coupled to the first control storage circuit and to the second control storage circuit for selecting one of the first and second control storage circuits based upon which one of the first and second interconnect masters is requesting an access to the shared storage. The prefetch circuitry can then use the selected control storage circuit to determine a prefetch operation triggered by the access to the shared storage.

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L6: Entry 5 of 66 File: PGPB Nov 11, 2004

DOCUMENT-IDENTIFIER: US 20040225758 A1
TITLE: Prefetch control in a data processing system

Detail Description Paragraph:
[0010] One embodiment of the present invention relates to selective prefetch control within a data processing system. For example, within a multi-master data processing system, prefetch operations may be triggered by an access request (e.g. a read access request, also referred to as a demand fetch) by a master based on such attributes as, for example, the identity of the master making the access request and the type of access request (e.g. whether the access request is for data or instruction or whether the access request is a burst or non-burst access). The prefetch operations can be determined or controlled through the use of a prefetch control register (or other prefetch control storage circuitry) capable of storing prefetch control information associated with, for example, each master within the data processing system. In some embodiments, a prefetch operation may include inhibiting prefetch such that no prefetch occurs. By selectively controlling prefetch within the data processing system, wasted prefetches, which consume excess power and result in lower performance, can be prevented.

Detail Description Paragraph:
[0012] Another embodiment of the present invention relates to a method for providing prefetch control in a data processing system. In this embodiment, an access request to access storage is received, a prefetch control storage circuit is provided to store prefetch burst access control information, and a prefetch to the storage is selectively initiated based upon the burst access control information and whether the access request is a burst access.

Detail Description Paragraph:
[0023] Still referring to FIG. 1, prefetch circuitry 40 can selectively control prefetching into buffers 42 based on control register 38. For example, in one embodiment, prefetch circuitry 40 determines, based on control register 38, a prefetch operation triggered by an access request to memory array 35 from a requesting master (such as master 12 or 14). Therefore, different types of prefetch operations can be triggered by different types of access attributes, which may include, for example, which master is requesting the access, whether the access request is part a burst access or not, whether the access request is for data or instructions, or any combination thereof. Therefore, based on the values of master identifier 26, R/W signal 38, burst signal 30, and instruction/data signal 32 corresponding to a current access request (i.e. a current demand fetch) and control register 38, prefetch circuitry 40 determines a prefetch operation that is triggered by the current access request.

Detail Description Paragraph:
[0028] In alternate embodiments, note that control register 38 may include more or less fields for each master with more or less bits, as needed. Also, the settings described in FIG. 3 for the fields of control register 38 are provided as an example. Alternate embodiments may determine prefetch operations triggered by either data access requests, instruction access requests, or both, based on different attributes than those provided in FIG. 3, more attributes that those of FIG. 3, or a subset of those in FIG. 3. For example, in one embodiment, prefetches

may be triggered based only on the identifier of the master currently requesting the access. Alternatively, prefetches may be triggered based only on whether the access request is a burst or non-burst access, regardless of the identifier of the master current requesting the access. Also note that in alternate embodiments, the particular attributes for a current access request can be indicated to prefetch circuitry 40 in a variety of ways other than by signals 28, 30, and 32 illustrated in FIG. 1.

CLAIMS:

12. A method for providing prefetch control, the method comprising: receiving an access request to access storage; providing a prefetch control storage circuit to store prefetch burst access control information; and selectively initiating a prefetch to the storage, based upon the burst access control information and whether the access request is a burst access.

14. A method as in claim 13, wherein the step of selectively initiating a prefetch to the storage comprises selectively initiating a prefetch to the storage, based upon the burst access control information, based upon whether the access request is a burst access, and based upon whether the access request is an instruction access or a data access.

18. A method as in claim 17, wherein the step of using control information stored in the prefetch storage circuit to control a prefetch operation triggered by the access request to the shared storage comprises selectively initiating a prefetch to the shared storage based upon whether the access request is a burst access.

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L6: Entry 19 of 66 File: USPT Nov 21, 2006

DOCUMENT-IDENTIFIER: US 7139878 B2
TITLE: Method and apparatus for dynamic prefetch buffer configuration and replacement

PRIOR-PUBLICATION:

DOC-ID	DATE
US 20040260908 A1	December 23, 2004

Description Paragraph (16):
Illustrated in FIG. 4 is an illustration of a status field 64 that represents by way of example only, any of the status fields illustrated in FIGS. 2 and 3. The status field 64 has an Address Tag Field or Tag Field, an Invalid Field or Invalid indicator, a Used Field or Used indicator, a Valid Field or Valid indicator, a Prefetched Field or Prefetched indicator, a Busy Bus Field or Busy Bus indicator and a Busy Fill Field or Busy Fill indicator. As was illustrated in FIGS. 3 and 4, the status field is associated with the smallest supported line size in the prefetch buffer 30. The Tag Field contains information that locates where in the prefetch buffer 30 a particular line of data is. The Invalid indicator denotes that the prefetch buffer 30 contains no valid data. In other words, the Invalid field indicates that a corresponding line of data in the prefetch buffer 30 is not valid. The Used indicator denotes that the prefetch buffer 30 contains valid data that has been provided to satisfy a bus burst type read. In other words, the Used field indicates that a corresponding line of data in the prefetch buffer 30 has been provided in response to a previous burst read request. The Valid indicator denotes that the prefetch buffer 30 contains valid data that has been provided to satisfy a bus single type (i.e. non-burst) read. In other words, the Valid field indicates a corresponding line in the prefetch buffer 30 has been provided in response to a previous non-burst read request. The Prefetched indicator denotes that the prefetch buffer 30 contains valid data that has been prefetched to satisfy a potential future bus access. The Busy Bus indicator denotes that the prefetch buffer 30 is currently being used to satisfy a bus burst read initiated by one of the bus masters. The Busy Fill indicator denotes that the prefetch buffer 30 has been allocated to receive data from a memory and the memory access is still in progress. The memory access may have been initiated by a preftch operation performed by prefetch control circuitry 32 and not directly associated with an access request from one of the bus masters. These indicators in status field 64 are used to determine which line or lines in prefetch buffer 30 are selected as a replacement entry. Selection of which line or lines to be chosen as a replacement entry is made in a prioritized order of the indicators of status field in the order of Invalid, Used, Valid, Prefetched, Busy Bus and Busy Fill as illustrated in FIG. 4. Note that alternate embodiments may use different indicators than those illustrated in FIG. 4 or may combine or encode indicators in an alternate manner.

CLAIMS:

7. The method of claim 6, wherein each of the status fields comprise an address tag field, an invalid field to indicate that a corresponding line in the prefetch buffer is not valid, a used field to indicate that a corresponding line in the prefetch buffer has been provided in response to a previous burst read request, and

a valid field to indicate a corresponding line in the prefetch buffer has been provided in response to a previous non-burst read request.

12. A method for configuring a prefetch buffer, comprising: receiving a read request to a memory from a requesting master, the read request having a corresponding data size and burst length; providing a prefetch buffer reconfiguration indicator based on the data size and the burst length; selecting a replacement entry within the prefetch buffer; based on the prefetch buffer reconfiguration indicator, selectively modifying a total length of the replacement entry of the prefetch buffer based on an attribute of the read request to an adjusted line size that eliminates dedicating unused buffer storage to the replacement entry of the prefetch buffer; and storing data fetched from the memory in the replacement entry.

18. A data processing system, comprising: a master; a memory; a prefetch buffer, coupled to the master and the memory, the prefetch buffer having a plurality of lines and status fields, each of the plurality of lines having a corresponding one of the status fields, each of the status fields comprises an address tag field, an invalid field to indicate that a corresponding line in the prefetch buffer is not valid, a used field to indicate that a corresponding line in the prefetch buffer has been provided in response to a previous burst read request, and a valid field to indicate a corresponding line in the prefetch buffer has been provided in response to a previous non-burst read request; and prefetch control circuitry coupled to the prefetch buffer, the prefetch control circuitry, in response to a read request from the master, selectively modifying a line size of at least a portion of the prefetch buffer.

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L6: Entry 24 of 66 File: USPT Mar 22, 2005

DOCUMENT-IDENTIFIER: US 6871246 B2
TITLE: Prefetch control in a data processing system

Detailed Description Text (4):
One embodiment of the present invention relates to selective prefetch control within a data processing system. For example, within a multi-master data processing system, prefetch operations may be triggered by an access request (e.g. a read access request, also referred to as a demand fetch) by a master based on such attributes as, for example, the identity of the master making the access request and the type of access request (e.g. whether the access request is for data or instruction or whether the access request is a burst or non-burst access). The prefetch operations can be determined or controlled through the use of a prefetch control register (or other prefetch control storage circuitry) capable of storing prefetch control information associated with, for example, each master within the data processing system. In some embodiments, a prefetch operation may include inhibiting prefetch such that no prefetch occurs. By selectively controlling prefetch within the data processing system, wasted prefetches, which consume excess power and result in lower performance, can be prevented.

Detailed Description Text (6):
Another embodiment of the present invention relates to a method for providing prefetch control in a data processing system. In this embodiment, an access request to access storage is received, a prefetch control storage circuit is provided to store prefetch burst access control information, and a prefetch to the storage is selectively initiated based upon the burst access control information and whether the access request is a burst access.

Detailed Description Text (17):
Still referring to FIG. 1, prefetch circuitry 40 can selectively control prefetching into buffers 42 based on control register 38. For example, in one embodiment, prefetch circuitry 40 determines, based on control register 38, a prefetch operation triggered by an access request to memory array 35 from a requesting master (such as master 12 or 14). Therefore, different types of prefetch operations can be triggered by different types of access attributes, which may include, for example, which master is requesting the access, whether the access request is part a burst access or not, whether the access request is for data or instructions, or any combination thereof. Therefore, based on the values of master identifier 26, R/W signal 38, burst signal 30, and instruction/data signal 32 corresponding to a current access request (i.e. a current demand fetch) and control register 38, prefetch circuitry 40 determines a prefetch operation that is triggered by the current access request.

Detailed Description Text (22):
In alternate embodiments, note that control register 38 may include more or less fields for each master with more or less bits, as needed. Also, the settings described in FIG. 3 for the fields of control register 38 are provided as an example. Alternate embodiments may determine prefetch operations triggered by either data access requests, instruction access requests, or both, based on different attributes than those provided in FIG. 3, more attributes that those of FIG. 3, or a subset of those in FIG. 3. For example, in one embodiment, prefetches

may be triggered based only on the identifier of the master currently requesting the access. Alternatively, prefetches may be triggered based only on whether the access request is a burst or non-burst access, regardless of the identifier of the master current requesting the access. Also note that in alternate embodiments, the particular attributes for a current access request can be indicated to prefetch circuitry 40 in a variety of ways other than by signals 28, 30, and 32 illustrated in FIG. 1.

CLAIMS:

12. A method for providing prefetch control, the method comprising: receiving an access request to access storage; providing a prefetch control storage circuit to store prefetch burst access control information; and selectively initiating a prefetch to the storage, based upon the burst access control information and whether the access request is a burst access.

14. A method as in claim 13, wherein the step of selectively initiating a prefetch to the storage comprises selectively initiating a prefetch to the storage, based upon the burst access control information, based upon whether the access request is a burst access, and based upon whether the access request is an instruction access or a data access.

17. A method for providing prefetch control in a data processing system, the method comprising: providing a first interconnect master; providing a second interconnect master; receiving an access request to access shared storage; selecting a prefetch control storage circuit based upon whether the access request is from the first interconnect master or the second interconnect master; using control information stored in the prefetch storage circuit to control a prefetch operation triggered by the access request to the shared storage, wherein using the control information stored in the prefetch storage circuit to control the prefetch operation triggered by the access request to the shared storage comprises selectively initiating a prefetch to the shared storage based upon whether the access request is a burst access.

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